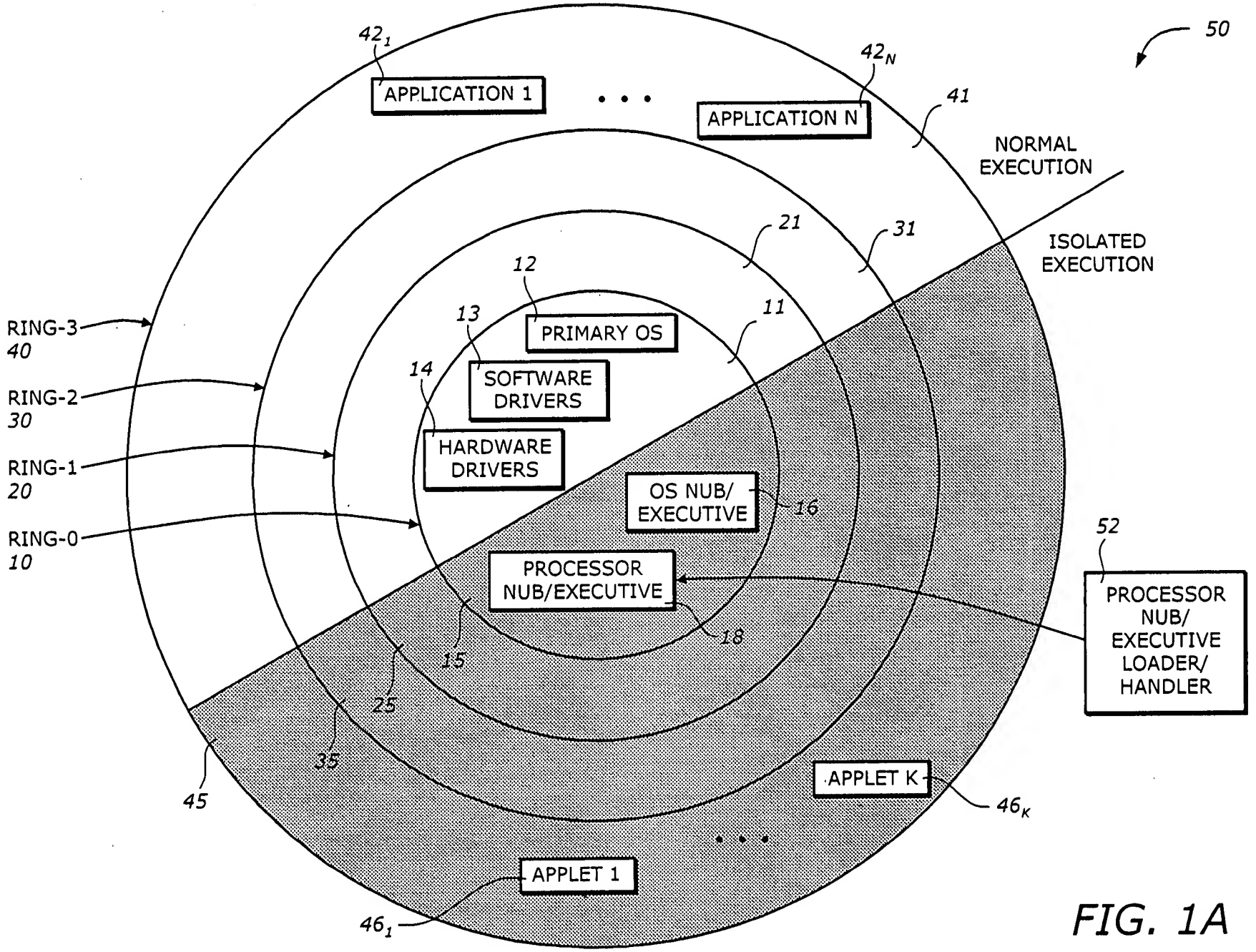


FIG. 1A

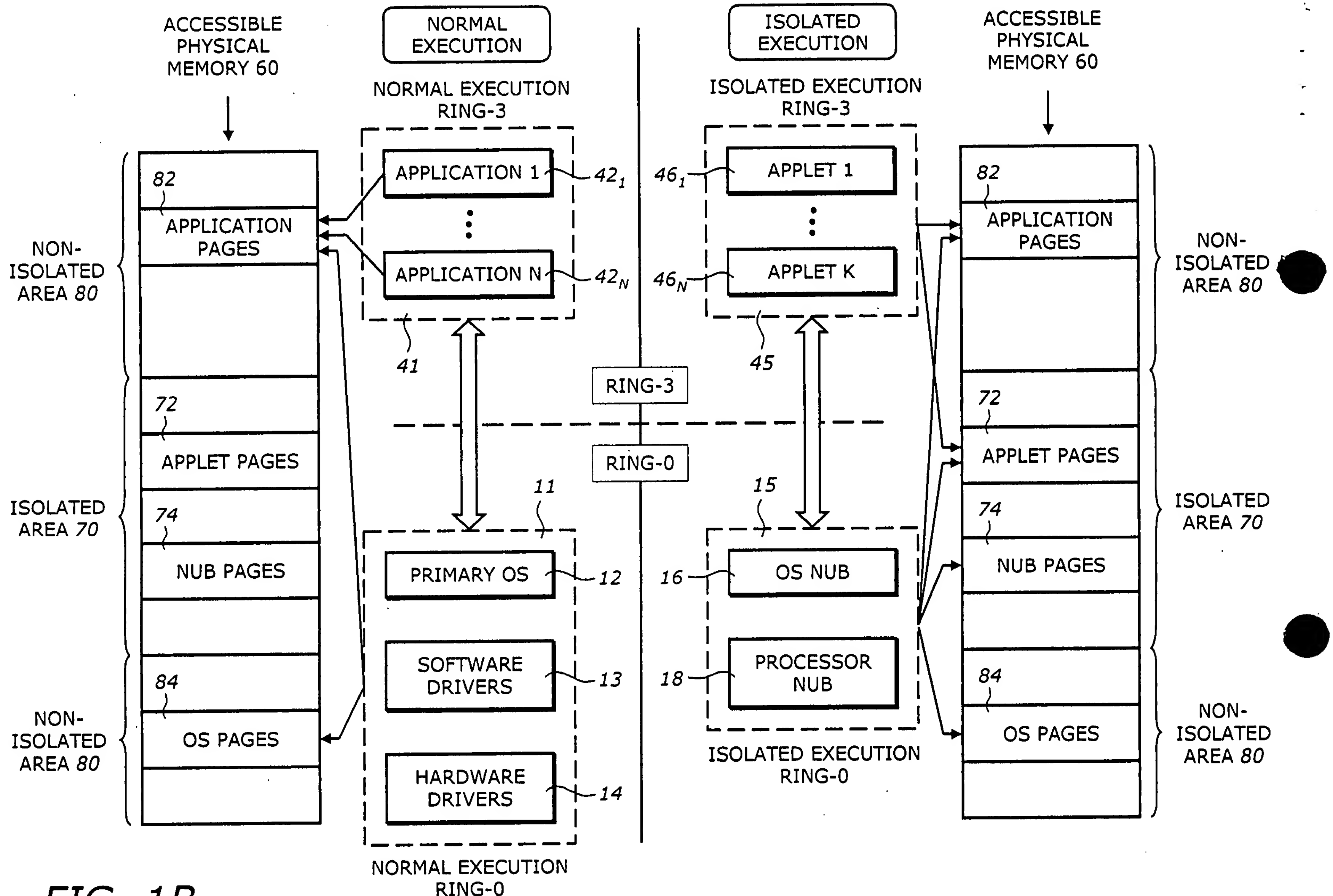

ACCESSIBLE PHYSICAL MEMORY 60
NORMAL EXECUTION
NORMAL EXECUTION RING-3
ISOLATED EXECUTION
ISOLATED EXECUTION RING-3
ACCESSIBLE PHYSICAL MEMORY 60
82
APPLICATION PAGES
APPLICATION 1
42₁
46₁
APPLET 1
APPLICATION N
42N
46N
APPLET K
NON-ISOLATED AREA 80
41
45
RING-3
RING-0
72
APPLET PAGES
ISOLATED AREA 70
74
NUB PAGES
11
15
PRIMARY OS
12
16
OS NUB
SOFTWARE DRIVERS
13
18
PROCESSOR NUB
84
OS PAGES
HARDWARE DRIVERS
14
ISOLATED EXECUTION RING-0
NORMAL EXECUTION RING-0

FIG. 1B

09895451 . 030301

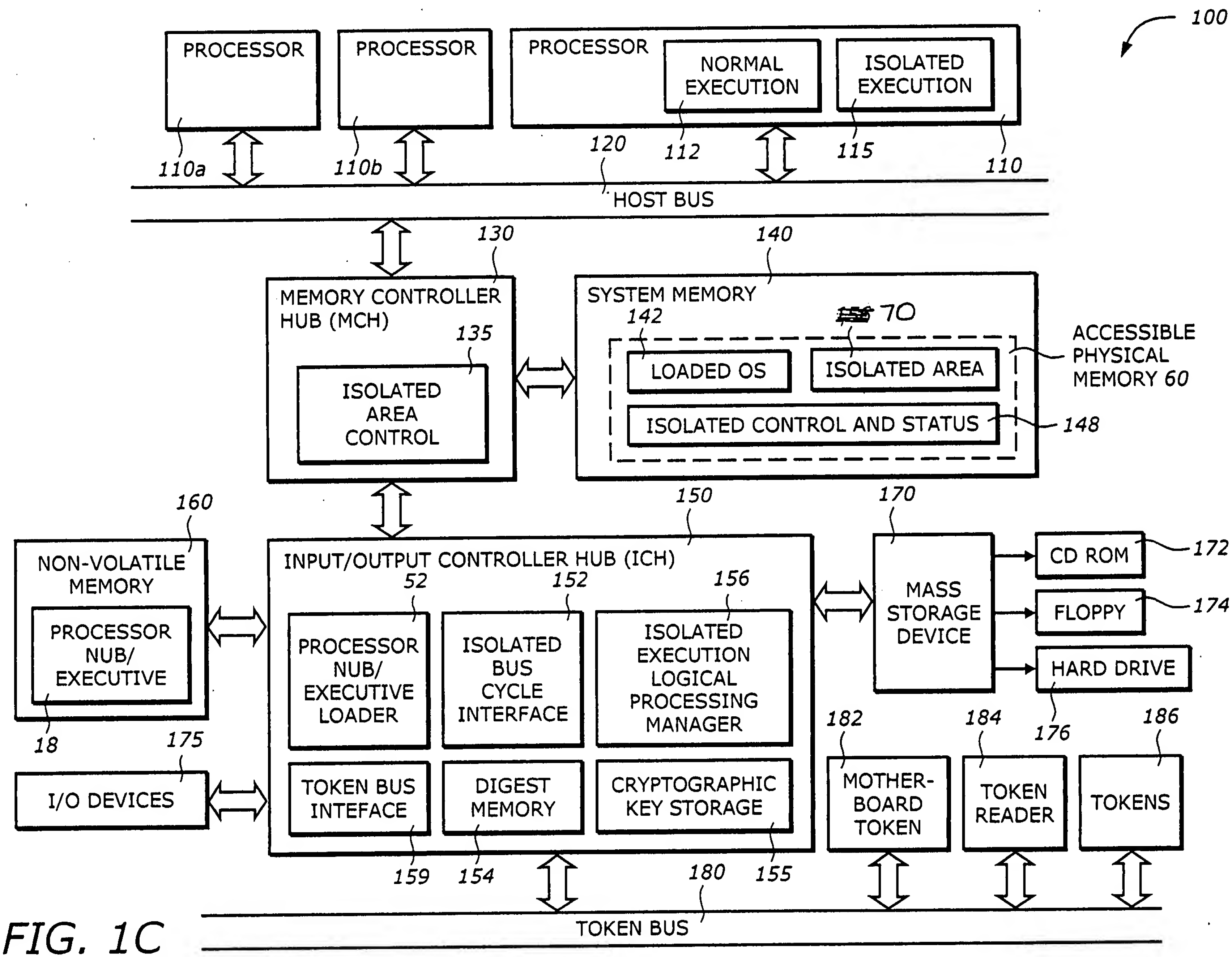


FIG. 1C

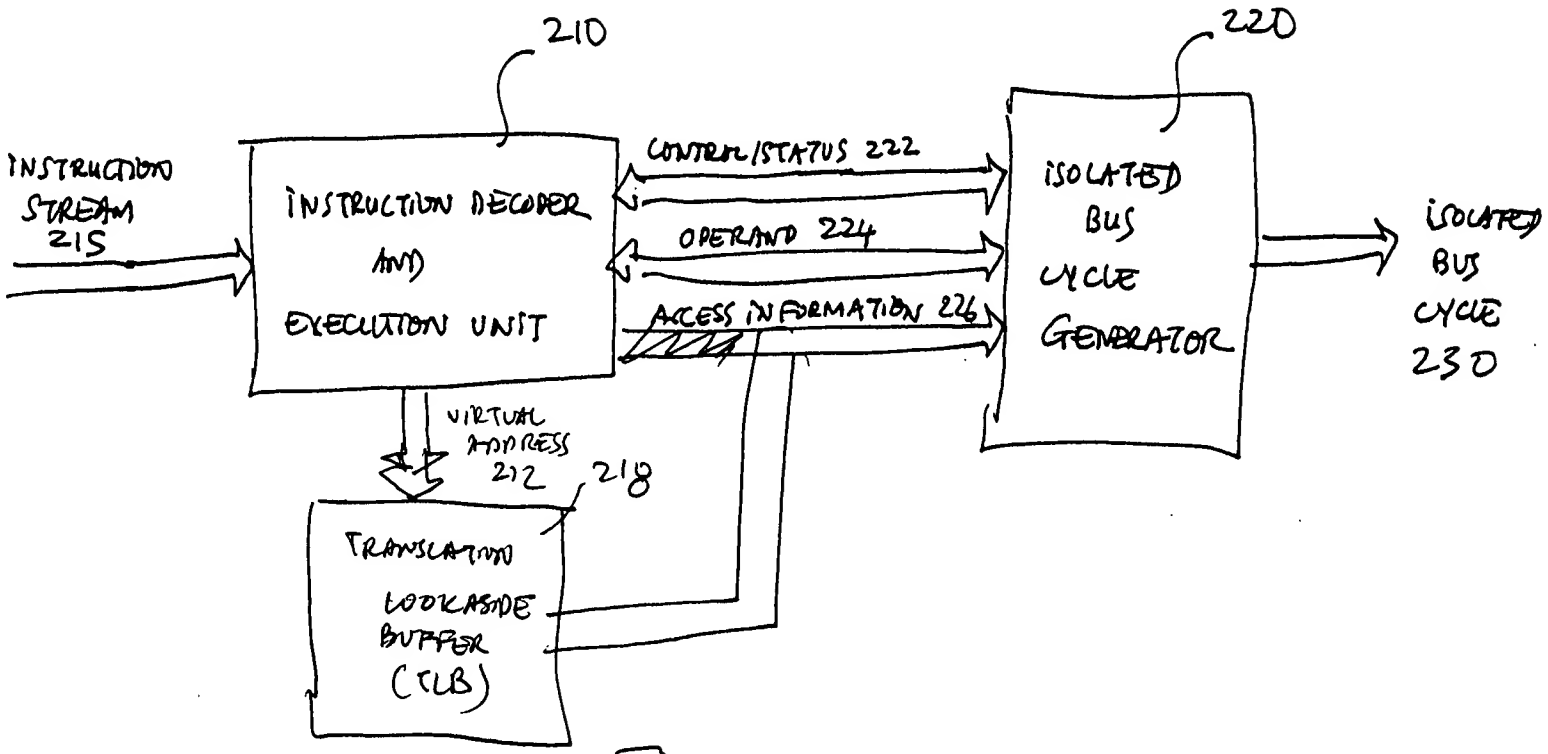


FIG. 2A

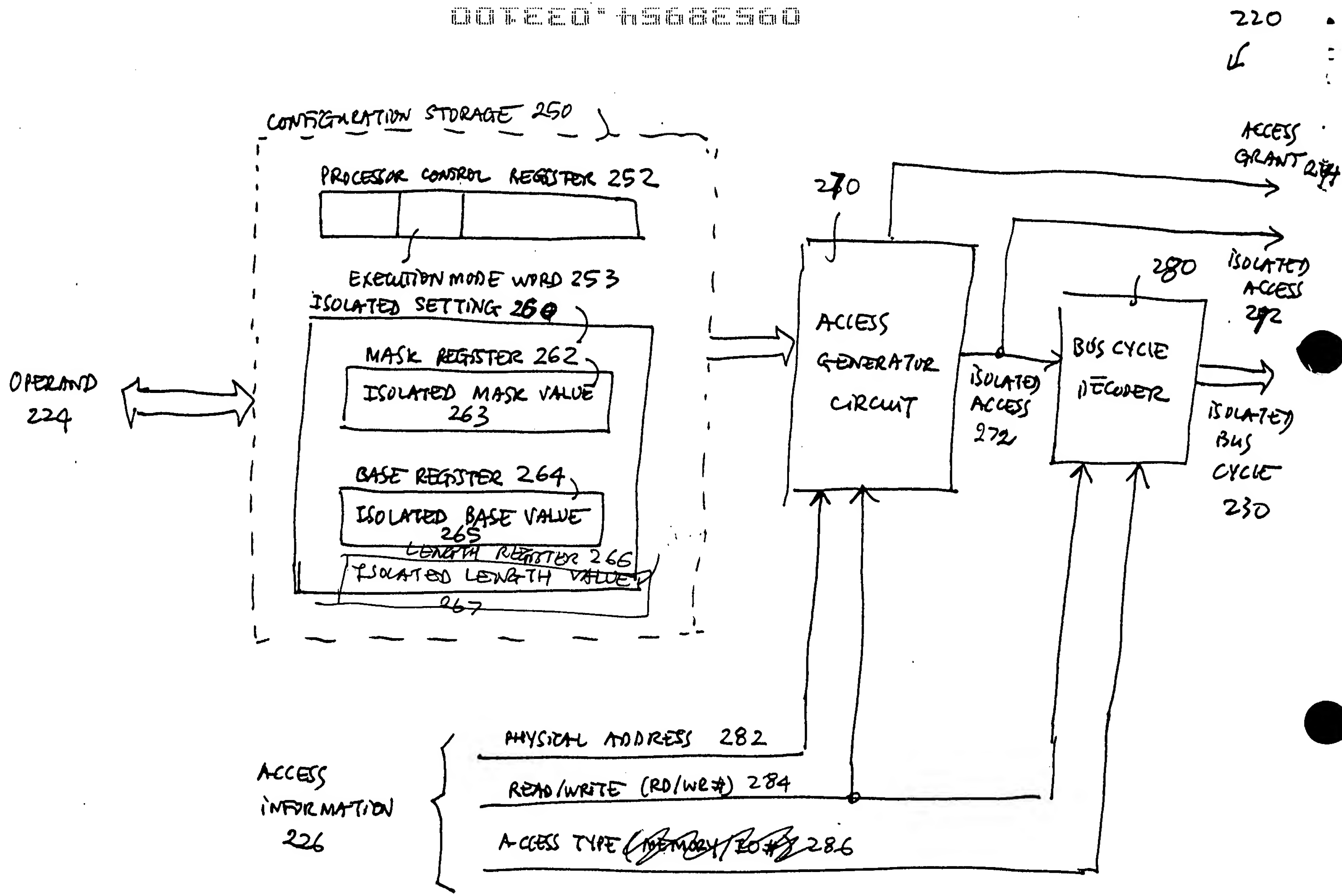

220
CONFIGURATION STORAGE 250
PROCESSOR CONTROL REGISTER 252
EXECUTION MODE WORD 253
ISOLATED SETTING 260
MASK REGISTER 262
ISOLATED MASK VALUE 263
BASE REGISTER 264
ISOLATED BASE VALUE 265
LENGTH REGISTER 266
ISOLATED LENGTH VALUE 267
OPERAND 224
270
ACCESS GENERATOR CIRCUIT
ISOLATED ACCESS 272
280
BUS CYCLE DECODER
ACCESS GRANT 294
ISOLATED ACCESS 292
ISOLATED BUS CYCLE 230
PHYSICAL ADDRESS 282
READ/WRITE (RD/WR#) 284
ACCESS TYPE (MEMORY/IO#) 286
ACCESS INFORMATION 226

FIG. 2B

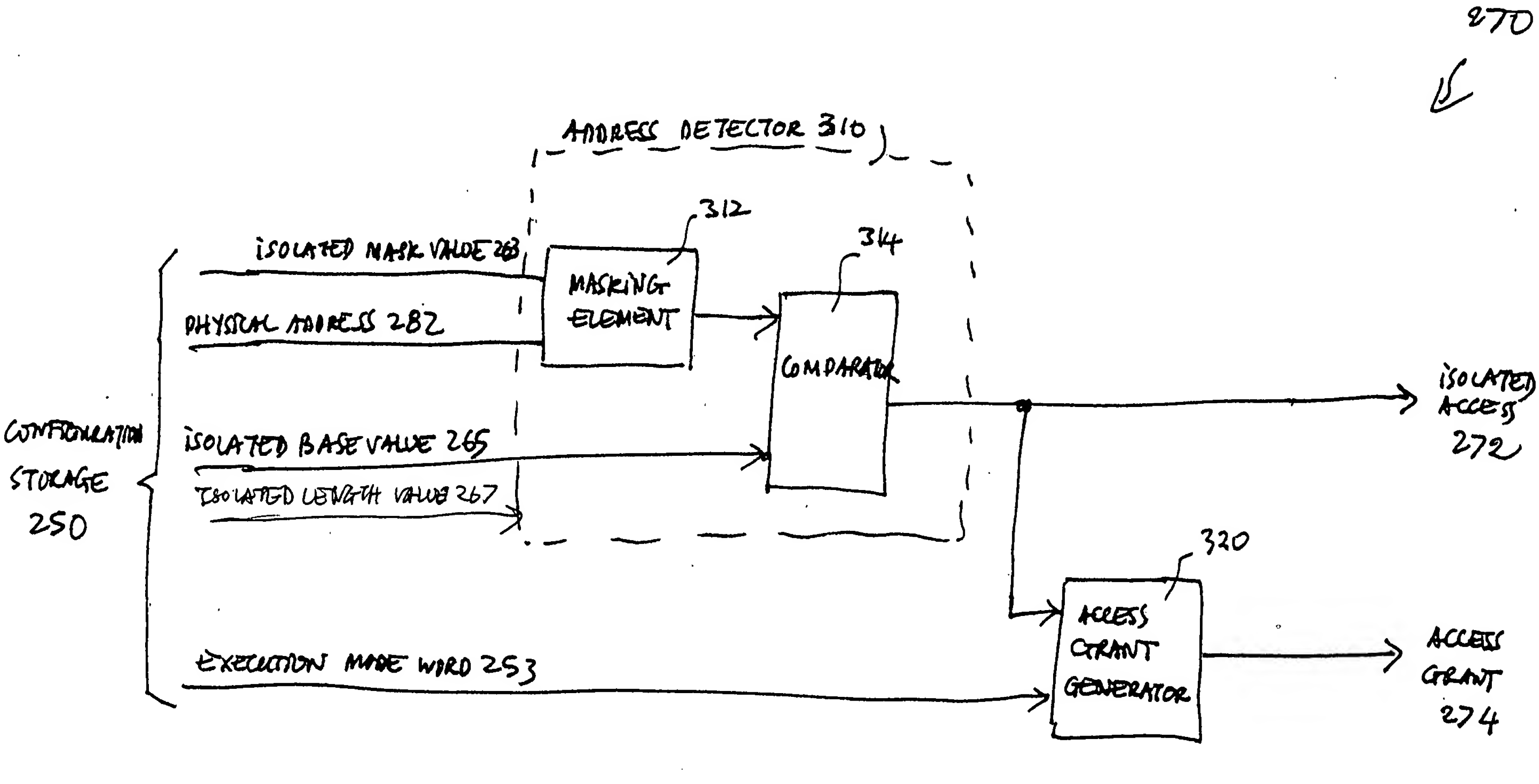
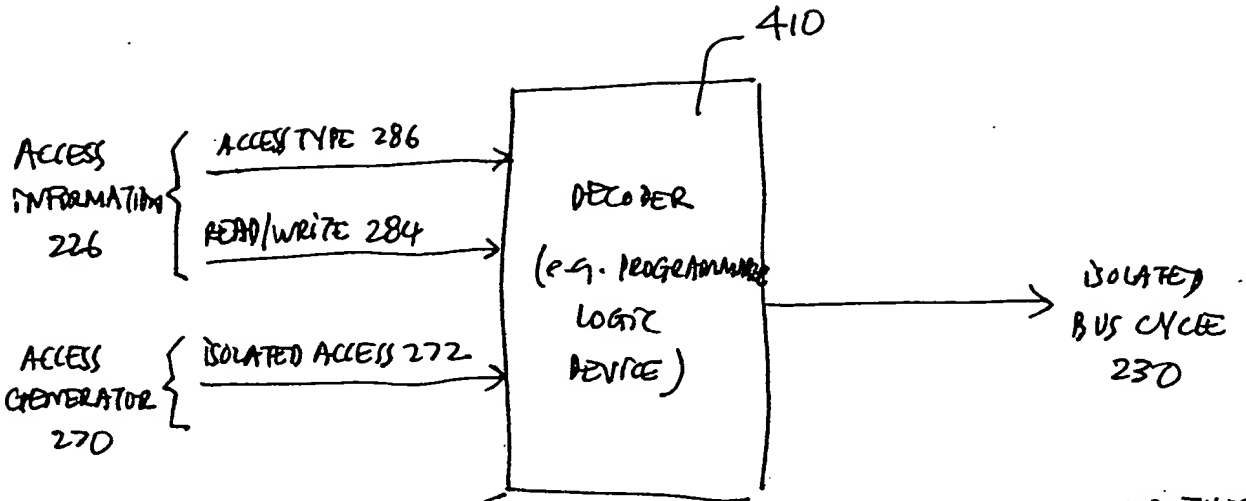


FIG. 3



TRUTH TABLE 420

ACCESS TYPE			ISOLATED ACCESS	ISOLATED BUS CYCLE		RING LEVEL
ISOLATED ENABLED STATE	M/IO#	RD/WR#				
X	X	X	DE-ASSERTED	NOT AVAILABLE		0
ENTRY (e.g., ISO_INIT)	X	X	ASSERTED	THREAD ENTRY	THREAD CYCLE	0
WITHDRAW (e.g., ISO_CLOSE)	X	X	ASSERTED	THREAD WITHDRAWAL		0
X	MEMORY REFERENCE	READ	ASSERTED	ISOLATED DATA READ	DATA ACCESS CYCLE	0
X	MEMORY REFERENCE	WRITE	ASSERTED	ISOLATED DATA WRITE		0
X	I/O REFERENCE	READ	ASSERTED	ISOLATED CONTROL READ	CONTROL ACCESS CYCLE	0
X	I/O REFERENCE	WRITE	ASSERTED	ISOLATED CONTROL WRITE		0

FIG. 4

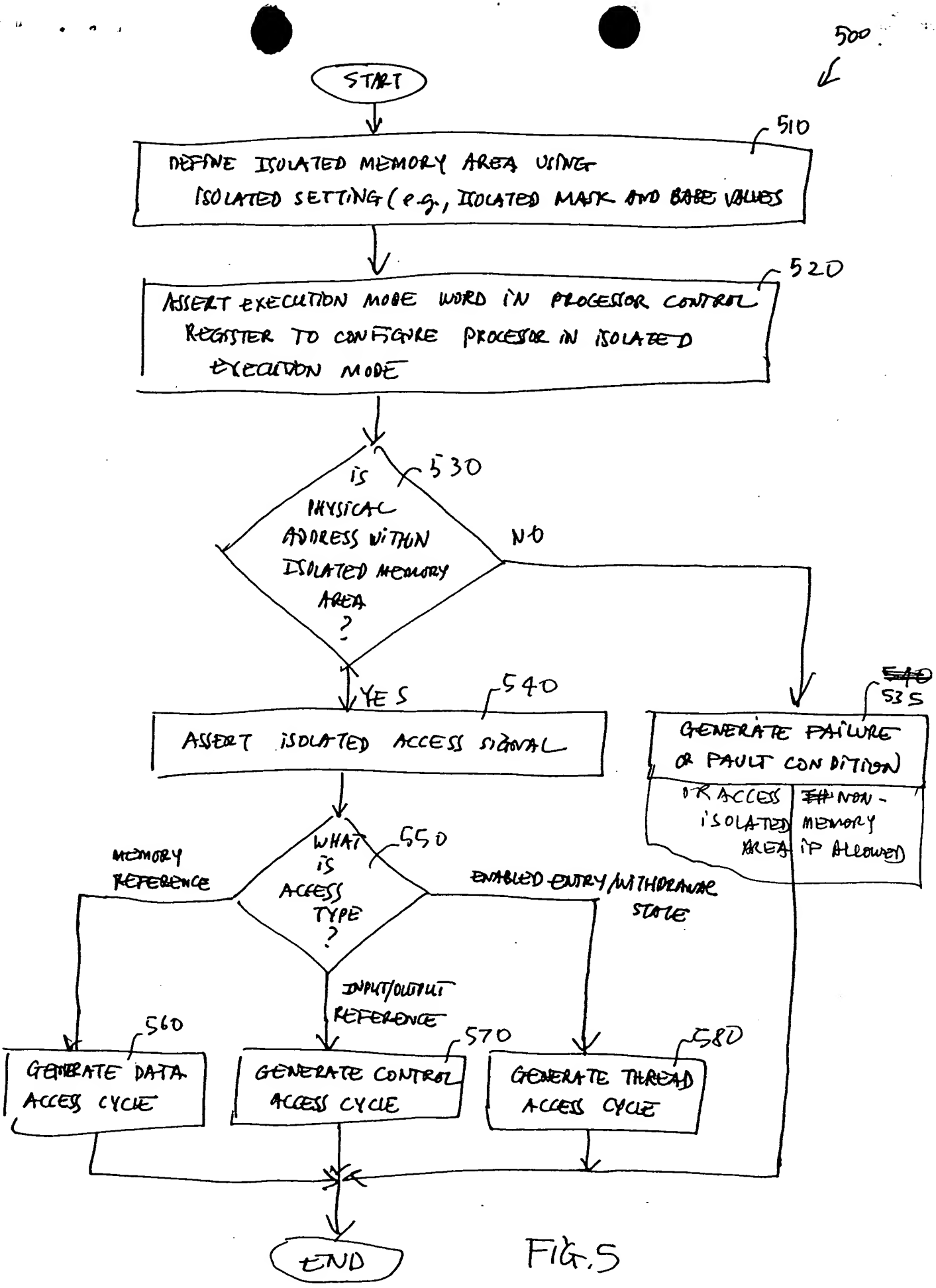

500
START
510
DEFINE ISOLATED MEMORY AREA USING ISOLATED SETTING (e.g., ISOLATED MASK AND BASE VALUES
520
ASSERT EXECUTION MODE WORD IN PROCESSOR CONTROL REGISTER TO CONFIGURE PROCESOR IN ISOLATED EXECUTION MODE
530
IS PHYSICAL ADDRESS WITHIN ISOLATED MEMORY AREA ?
NO
YES
540
ASSERT ISOLATED ACCESS SIGNAL
535
GENERATE FAILURE OR FAULT CONDITION
OR ACCESS ISOLATED NON-MEMORY AREA IF ALLOWED
550
WHAT IS ACCESS TYPE ?
MEMORY REFERENCE
INPUT/OUTPUT REFERENCE
ENABLED ENTRY/WITHDRAWAL STATE
560
GENERATE DATA ACCESS CYCLE
570
GENERATE CONTROL ACCESS CYCLE
580
GENERATE THREAD ACCESS CYCLE
END

FIG. 5